AMENDMENTS TO THE CLAIMS

1. (Currently amended) A detector for detecting states of a plurality of jacks, each jack comprising a first switch having a first normally closed terminal and a first output terminal, and a second switch having a second normally closed terminal and a second output terminal, the detector comprising:

a plurality of bias resistors each coupled to one of the first output terminals, respectively;

a control unit for determining the states of the plurality of jacks; and

a plurality of matching resistors each coupled to one of the second output terminals, respectively, so as to match with an output resistance of the first and the second switches of the plurality of jacks;

wherein the first normally closed terminals are commonly coupled to a first node and the control unit determines the states of the plurality of jacks according to a voltage at the first node.

2. (Original) The detector according to claim 1 further comprising:

a pull-up resistor having a first terminal coupled to a power source, and a second terminal coupled to the first node.

3. (Original) The detector according to claim 1 wherein the control unit comprises:

a converter for outputting a decoding signal according to the voltage at the first node; and

a decoder for receiving the decoding signal and decoding the decoding signal into a corresponding state signal, which indicates the state of each of the jacks;

wherein resistances of the bias resistors are configured such that a value of the decoding

signal corresponds to the states of the jacks.

4. (Original) The detector according to claim 3, wherein the converter is an analog-to-digital converter.

5. (Original) The detector according to claim 1, further comprising a plurality of adjusting resistors through each of which one of the first normally closed terminals are coupled to the first node, respectively.

6. (Original) The detector according to claim 1, further comprising:

a filter capacitor coupled to the first node; and

a filter resistor coupled between the commonly coupled first normally closed terminals and the first node.

Claim 7 (Cancelled)

8. (Original) The detector according to claim 1, wherein the bias resistors have different resistances.

9. (Original) The detector according to claim 8, wherein the bias resistors have resistances sequenced in a geometric progression having a common ratio of 2.

10. (Currently Amended) A detector for detecting states of a plurality of jacks, each jack comprising a first switch having a first normally closed terminal and a first output terminal and a second switch having a second normally closed terminal and a second output terminal, when there is no external terminal being inserted into a jack, the first normally closed terminal of the jack is coupled to the first output terminal of the jack and the second normally closed terminal of the jack is coupled to the second output terminal of the jack, and when there is an external terminal being inserted into the jack, the first normally closed terminal of the jack is not coupled to the first output terminal of the jack and the second normally closed terminal of the jack is not coupled to the second output terminal of the jack, the detector comprising:

a plurality of bias resistors each coupled to one of the first output terminals, respectively;

a control unit for determining the states of the plurality of jacks; and

a plurality of matching resistors each coupled to one of the second output terminals, respectively, so as to match with an output resistance of the first and the second switches of the plurality of jacks;

wherein the first normally closed terminals are commonly coupled to a first node and the control unit determines the states of the plurality of jacks according to a voltage at the first node.

11. (Original) The detector according to claim 10 further comprising:

a pull-up resistor having a first terminal coupled to a power source, and a second terminal coupled to the first node.

12. (Original) The detector according to claim 10 wherein the control unit comprises:

a converter for outputting a decoding signal according to the voltage at the first node; and

a decoder for receiving the decoding signal and decoding the decoding signal into a corresponding state signal, which indicates the state of each of the jacks;

wherein resistances of the bias resistors are configured such that a value of the decoding signal corresponds to the states of the jacks.

13. (Original) The detector according to claim 10, further comprising a plurality of adjusting resistors through each of which one of the first normally closed terminals are coupled to the first node, respectively.

14. (Original) The detector according to claim 10, further comprising:

a filter capacitor coupled to the first node; and

a filter resistor coupled between the commonly coupled first normally closed terminals and the first node.

Claim 15 (Cancelled)

16. (New) A detector for detecting states of a plurality of jacks, each jack comprising a first switch having a first normally closed terminal and a first output terminal, the detector comprising:

a plurality of bias resistors each coupled to one of the first output terminals, respectively;

a control unit for determining the states of the plurality of jacks; and

a plurality of adjusting resistors through each of which one of the first normally closed terminals is coupled to a first node, respectively;

wherein the first normally closed terminals are commonly coupled to the first node, and the control unit determines the states of the plurality of jacks according to a voltage at the first node.

17. (New) The detector according to claim 16, wherein the control unit comprises:

a converter for outputting a decoding signal according to the voltage at the first node; and

a decoder for receiving the decoding signal and decoding the decoding signal into a corresponding state signal, which indicates the state of each of the jacks.

18. (New) The decoder according to claim 16, wherein the bias resistors have different resistances.

19. (New) The decoder according to claim 18, wherein the bias resistors have resistances sequenced in a geometric progression having a common ratio of 2.

20. (New) A detector for detecting states of a plurality of jacks, each jack comprising a first switch having a first normally closed terminal and a first output terminal, the detector comprising:

a plurality of bias resistors each coupled to one of the first output terminals, respectively;

a control unit for determining the states of the plurality of jacks; and

a filter capacitor coupled to a first node, and a filter resistor coupled between the commonly coupled first normally closed terminals and the first node;

wherein the first normally closed terminals are commonly coupled to the first node, and the control unit determines the states of the plurality of jacks according to a voltage at the first node.

21. (New) The detector according to claim 20, wherein the control unit comprises:

a converter for outputting a decoding signal according to the voltage at the first node; and

a decoder for receiving the decoding signal and decoding the decoding signal into a corresponding state signal, which indicates the state of each of the jacks.

22. (New) The decoder according to claim 20, wherein the bias resistors have different resistances.

23. (New) The decoder according to claim 22, wherein the bias resistors have resistances sequenced in a geometric progression having a common ratio of 2.